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Modesat Communications 1024QAM Modem IP Core Product Description

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1. Overview

Modesat 1024QAM modulator/demodulator IP Core with PilotSync™ technology is designed for point-to-point microwave applications for backhaul, broadcasting and trunking segments. It is single carrier QAM modem with Dual-Polarization XPIC version due in Q3 2010. Modem can be evaluated and tested on provided PCB board (EVB) with Altera Cyclone III EP3C55 FPGA. For evaluation purposes Modesat offers time-limited version what must be connected to USB port via FPGA download cable during all evaluation period.

Two EVBs with 1024QAM Evaluation IP Core are used in back to back mode for verifying performance and parameters over a full duplex communications link. Onboard mixer and local oscillator allow matching intermediate frequency of the EVB output to ODU/external measuring equipment.

Data can be generated internally with PBER tester or provided by user. External interfaces are GbE for packet based transfers or CMI/HDB3 daughter board connected to EVB extension port for TDM data.

Modem core is controlled via USB interface (USB/serial) or RS232 terminal. Former allows to read/write register space and also to capture data from crucial internal points (equalizer, demapper aso). GUI program provided with EVB displays constellation diagrams and spectral plots. It also programs EVB into different configurations with minimal user intervention.

2. Features

The main features of the 1024QAM IP Core are listed below:

- I/Q baseband, complex IF or real IF interface
- Modulation: QPSK to 1024QAM (with adaptive switching)
- Roll-Off factor: software configurable 16-25%
- Bandwidth: software configurable 7 to 112MHz
- Symbol rate: software configurable 5-104 MSym/s
- PilotSync™ technology for fast carrier recovery
- Reed-Solomon FEC (204, ACM defined data size)
 - Soft-Decision LDPC in Q4 2010
- Interleaver/Deinterleaver depth: I = 12
- Single external analogue loop for AGC 18 bits
- Input from ADC: 11-12 bits (1 or 2 (I/Q) channels)
- Output to DAC: 10-16 bits (1 or 2 (I/Q) channels)
- Decision Feedback Equalizer in the receiver channel
- Shape Filter: Root-Raised-Cosine with 28 x N taps
 - N is the interpolation and decimation coefficient, in the case of 28MHz channel bandwidth, N=4 and the total number of taps is 112 in each channel with 12 bit coefficients in RX and 9-12 bit coefficients in TX channels

EVB evaluation encapsulates IP core with test and IO adding the following features:

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- IF software configurable from 70 to 1200 MHz in 2.5 MHz steps
- Transport stream is a multiplex of SDH, PDH and Gbit Ethernet data sources
- Configuration via host interface (USB/RS232)
- Modem master clock / sampling rate: single, fixed 200 or 210MHz XO clock source
- Internal calibrated AWGN generator, Knuth polar method/physical random white noise source
- Internal random data generator: PRBS generator with period of $2^{23} - 1$
- Internal BER tester

3. Supported data rates

The maximum supported transport stream data rate can be calculated according to the following formula:

$$F_{data} = F_{sym} * \langle bits\ per\ symbol \rangle / \langle coding\ overhead \rangle / \langle framing\ overhead \rangle$$

Where:

- Coding overhead is 1.0851 for Reed-Solomon 188/204 coding
- Framing overhead is 1.007

Depending on the target customer modem realization, a „wayside channel“ can be defined, that reserves a part of data bandwidth and makes it available on a separate data interface for implementing custom FEC/Interleaver solutions.

Example data rates:

Modulation	Bandwidth MHz	Symbol rate MHz	Data rate Mbit/s
1024QAM	112	97.2	889
1024QAM	56	48.6	444
512QAM	112	97.2	800
512QAM	56	48.6	400
256QAM	112	97.2	710
256QAM	56	48.6	355
128QAM	112	97.2	622
128QAM	56	48.6	306

With 200MHz master clock frequency and 200MHz MSPS ADC, symbol rates up to 99.995 MHz can be used (and its $1/2^n$ fractions). For symbol rates above and equal to 100/50/25/... a 210MHz master clock oscillator and consequently a 210MSPS ADC must be used.

4. Functional Description

4.1. Block Diagram

The functional block diagram below shows all functionality that is implemented in the EVB, the IP core part comprises functionality in the central part of the figure 1.

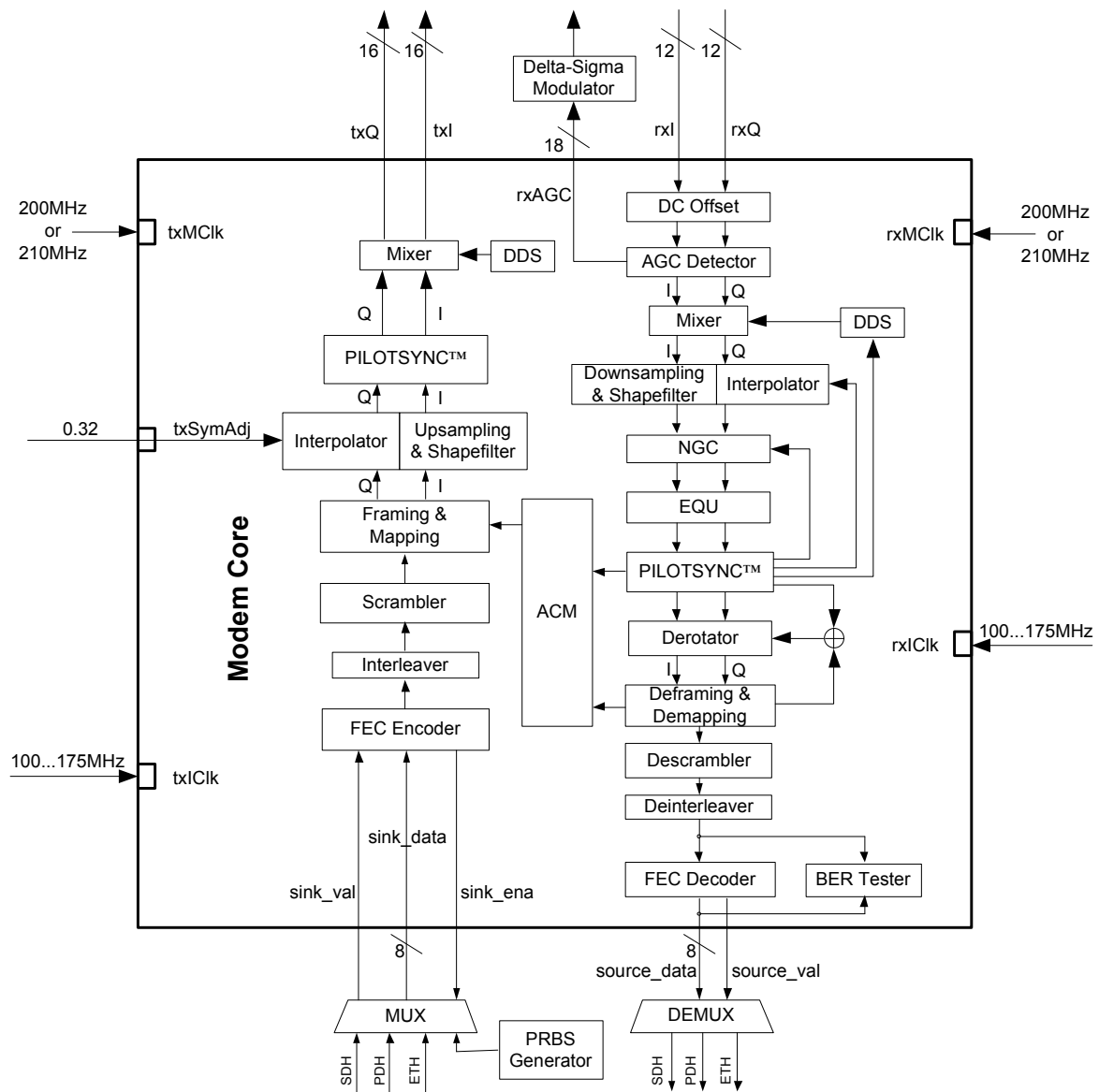


Fig.1. 1024QAM IP Modem Core

4.2. 1024QAM IP Modem Core Description of Operation

4.2.1. Modulator input bus and framing logic

Modem core works on the basis of a fixed frequency master clock representing output sample rate and an interface clock on which user data interfaces are based. The master clock should be generated by a fixed frequency XO and it must have a frequency at least 2x higher than the highest symbol rate that modem should support. A 200MHz master clock allows symbol rates up to 100MHz. To achieve higher symbol rates e.g. 104MHz, a 210MHz XO can be used.

The modulator input data bus is subset of Avalon-ST input bus to the Reed-Solomon FEC encoder. The timing of data transfers is governed by the physical layer framing logic. Data transfers take place in the form of 188 byte packets, which form the data part of a Reed-Solomon codeword. The number of these 188 byte packets that are collected together to form one physical layer frame depends on the modulation used. From QAM1024 down to QAM16 physical frame consists of 20...8 Reed Solomon codewords. This maintains the same physical layer frame length in symbols. All physical layer frames start with a 23 symbol header what is used for equalizer training in zero-forcing mode and high reliability message channel for ACM.

If it is desired that main Reed-Solomon encoded data channel only uses a portion of the physically available bandwidth then framing logic can include a number of „wayside“ symbols in every physical frame. This forms a separate raw data channel (“wayside channel”), representing available excess bandwidth. The number of wayside symbols per physical frame can be configured with 0,5 symbol accuracy, but the number of symbols that can actually be used for wayside data traffic can only be an even multiple of 16 symbols. For example if user wants to use QAM256 modulation with 469 symbols of wayside traffic per physical frame (typical for Reed-Solomon encoded STM-1 bitstream modulated into a 28MHz channel using 18% roll-off factor), the structure of the physical frame will contain:

- 23 symbols for PL header
- 3264 symbols for 16 R-S codewords
- 464 symbols of wayside traffic available for client use
- 5 dummy, unusable wayside symbols

The number of wayside symbols can be configured via the registers accessible over the host interface bus. Refer to Fig.2.

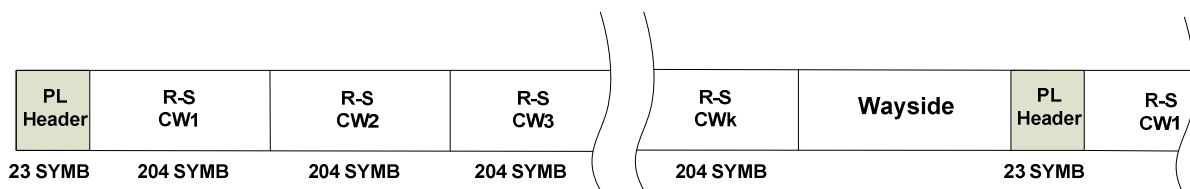


Fig.2. Structure of physical frame.

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This feature allows user to implement channels with custom error detection and interleaving. Provided evaluation platform contains multiplexer to transfer TDM data in fixed bandwidth channel leaving all remaining bandwidth to Ethernet packets.

4.2.2. Mapping

Reed-Solomon encoded and scrambled stream of bytes is sliced into symbols, each representing 10 or less bits, depending on the modulation used. The resulting unmapped symbols are then mapped onto actual constellations using a ROM-based mapper. Forced modulation type is configurable via GUI and automatic negotiated with ACM.

4.2.3. Upsampling and shaping filter

The modulated symbol stream will pass through a polyphase root-raised-cosine oversampling filter. The oversampling ratio which determines the channel bandwidth is set from registers accessible over the host interface bus.

Symbol rate related frequency response of this composite filter is equivalent to the 28 tap two times oversampling root-raised-cosine filter. Output of this filter becomes oversampled by an arbitrary factor, for example 4.13 for 28MHz bandwidth and 18% roll-off factor.

4.2.4. Modulator output and direct IF mixer

At its output, the modulator has a complex IF mixer with an associated DDS local oscillator, the base frequency of which can be set from configuration space. Modulator 16-bit I and Q outputs can be baseband outputs, with DDS set to 0 Hz or complex/real IF when DDS is operating at higher frequency. For real-IF applications single I or Q output is used.

4.2.5. Demodulator ADC input

The demodulator core works on the basis of a fixed frequency master clock that represents the input sample rate and an interface clock on which the data interfaces are based. The master clock should be generated by a fixed frequency XO and it must have a frequency at least 2x higher than the highest symbol rate the modem should support. A 200MHz master clock allows symbol rates up to 100MHz-50ppm. The master clock of the receiver is generally supplied by the ADC, in parallel with its data bus. The clock that drives the ADC is usually the same 200MHz or 210MHz clock used as the transmitter master clock.

Data is fed into the demodulator from I and Q channels with each having max 12 bits of resolution. For real IF sampling only one of I or Q inputs is used.

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4.2.6. Static complex baseband equalizer

The baseband equalizer is there to correct for the predictable channel frequency and phase response distortions caused by the imperfections in modulators, demodulators and ones that are caused by the design of analogue filters. It is mainly necessary for operation at wider bandwidths. Its coefficients are set from user space once after installation.

4.2.7. DC offset cancellation circuit

This circuit corrects the DC offset that stems from imperfections in circuit design and also corrects the near-DC fluctuations caused by the effects of AC coupling of baseband I and Q channels.

4.2.8. Demodulator analogue AGC detector and loop

The analogue AGC loop aims to keep the signal level at the input of the ADC low enough that it does not clip. The AGC digital loop filter output has 18 bits of resolution and is used for driving a second order delta-sigma modulator acting as single bit DAC. The output of this DAC is used to drive an analogue VGA.

4.2.9. Direct IF sampling mixer

The demodulator input I and Q channels are fed into a complex mixer together with a local oscillator signal that is produced by a DDS. During baseband I and Q operation, the base frequency of this DDS is configured to be 0Hz. When direct IF sampling (real or complex) is desired, the frequency of this DDS is configured to equal the RX IF frequency from control registers.

4.2.10. Downsampling and shaping filter

The baseband I and Q channel data is sent to polyphase root-raised-cosine downsampling filter. Downsampling ratio determining channel bandwidth is user configurable.

Symbol rate related frequency response of this composite filter is equivalent to that of the 28 tap RRC filter.

4.2.11. NGC

The NGC (numerical gain control) is an active element of the secondary automatic gain control loop which aims to keep the signal level at the input of the equalizer within acceptable range.

4.2.12. Equalizer

The equalizer evens out channel fluctuations and allows modem to operate in dynamic fading conditions. It operates in Zero-Forcing or Decision Feedback modes depending on the spectral notch parameters.

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ZF equalizer locks onto the physical layer framing structure and measures the impulse response of a channel based on physical layer frame headers. A DSP within the equalizer then calculates the filter coefficients necessary to counter the frequency and phase response non-linearities in channel. Decision feedback mode operates continuously and keeps resulting symbol centered in decision space.

4.2.13. Derotator

Equalized I and Q channels are fed into a phase correction complex mixer with a 0Hz local oscillator DDS. The phase of this local oscillator is controlled by the demapper described below.

4.2.14. PilotSync™ synchronizer

The synchronizer extracts and analyzes the pilot tones present in the signal and produces several control signals for coarse and fine carrier recovery, including:

- symbol (ADC) clock control signal that adjust the downsampling ratio of the Rx channel filter
- carrier frequency control signal that drives the baseband demixer
- level adjustment signal that drives the NGC

Parameters of all filter loops can be adjusted via the registers that are accessible over the host interface bus.

4.2.15. Deframing, demapping and demodulator data output

The deframing and demapping block converts received signals into binary symbols based on a constellation chosen via the host interface registers and slices them together. Resulting bytestream progresses through deinterleaver and is assembled into 204 byte codewords for Reed-Solomon error correction block. The output of the Reed-Solomon decoder forms the output of the PilotSync™ modem IP core.

Deframing logic also extracts the “wayside channel” from the main channel and outputs it on a separate data bus as direct byte stream.

4.2.16. Adaptive Coding and Modulation (ACM) Module

ACM raises overall system throughput and improves link quality with negotiating link partners to use highest mutually sustainable modulation rate at any given path conditions. It automatically up- and downshifts modulation between QPSK and 1024-QAM and chooses best coding ratio for FEC.

The Modesat 1024QAM IP Core physical layer framing structure includes a highly guarded, low bitrate service channel, which is used for transmitting modulation change requests and status information (MER and BER) from receiver to transmitter. Receiver side ACM module compares current path state with stored profile and upon match requests communicating parties to make synchronous modulation/coding

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rate switch. This switch occurs at both ends with no data loss and can change operating parameters once in half milliseconds.

4.2.17. FEC Reed-Solomon encoder/decoder

The Modesat 1024QAM IP Core uses the Reed-Solomon from Altera to in Standard encoder and Full bit error decoder configuration.

The Reed-Solomon encoder and decoder interfaces are based on the Avalon-ST interface specification. Alternative FEC options can be provided upon the request of the customer, however using other FECs will increase resource requirements.

4.2.17. External interfaces - 1000Mbps Ethernet MAC and TDM

Evaluation platform adds external data interface support to Modesat 1024QAM IP Core. TDM data can be communicated over radio link from CMI/HDB3 interfaces and packet switch networks via GbE.

In case single interface type is connected then source timing will be transferred from transmitter to receiver allowing to keep external data interfaces synchronized (SyncE, STM-1). If several standards need to be transmitted at once for hybrid solution then source clock must be selected from one of the sources and receiver side should use PLL-s to synchronize different time domain output channels.

For packet networks GbE Ethernet functionality to Modem Rx and Tx interfaces can be configured to work in bridging 1000Mbps Ethernet mode. When configured in Ethernet mode the 1000B-T/TX MAC functionality will be included in the same FPGA device with modem IP core. An external RGMII PHY interfaces data to network via 1000BASE-T magnetics. The Ethernet interface complies with the IEEE 802.3 standard supporting pause frame based flow control.

A modem pair equipped with Ethernet interfaces, works on Data Link Layer (Layer 2) in bridge mode – all incoming packets are forwarded to radio link partner and vice versa. The Ethernet MAC allows the user data interface to work in a packetized payload mode while the radio link is working in a streaming mode.

Data transfer subsystem in Modesat QAM modem can be enhanced with QoS filters and queue management as well as with header and data compression for throughput improvement.

4.3. 1024QAM IP Modem Core Input and Output signals

Fig. 3 below shows a high level view of the main blocks that comprise the IP Modem core, with focus on the input and output signals. These signals are further described in the paragraphs below.

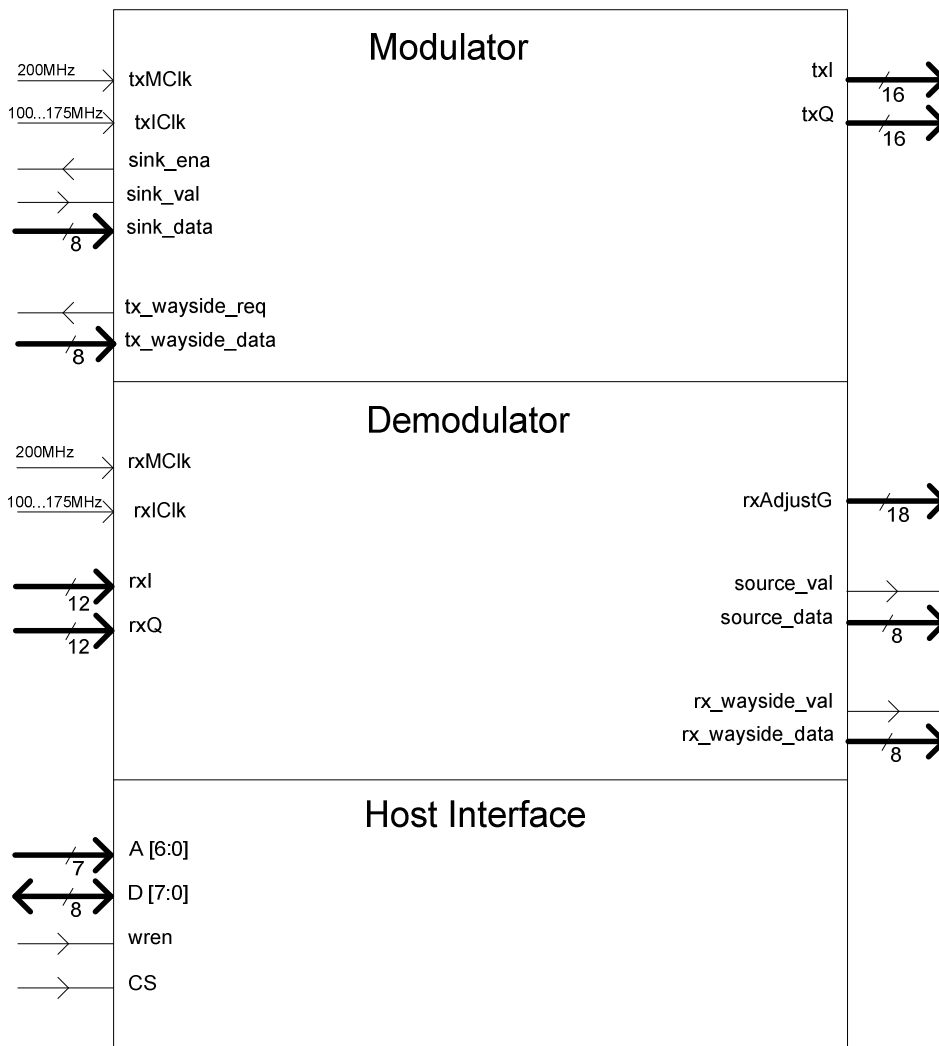


Fig.3. Modem Core.

4.3.1. Modulator (Transmit Side)

The modulator uses a separate clock for a data interfaces. The frequency can be between 100 and 175MHz. Ethernet implementation uses 125MHz as an interface clock, SDH interface 155.52MHz.

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Data bus follows Avallon Streaming interface standard. The **sink_ena** signal indicates that a modem is ready to receive a packet of data (Fig.4 below). The packet size is 188 bytes, i.e. one Reed-Solomon codeword before encoding. An asserted **sink_val** indicates that **sink_data** bus represents a valid data byte. The first byte must be provided within 12 symbol time periods (48 or 96 clock periods) of **sink_ena** going high. Data transmission on the sink_data/sink_val bus does not need to be continuous, it can be interrupted at any time by lowering **sink_val**. The average byte rate must however be at least equal to the transmission bandwidth.

After the last byte of a 188byte packet has been received by the modem, it lowers the **sink_ena** signal, indicating that it is not ready to accept any more data. It will assert **sink_ena** again when there is enough room in the transmit buffer.

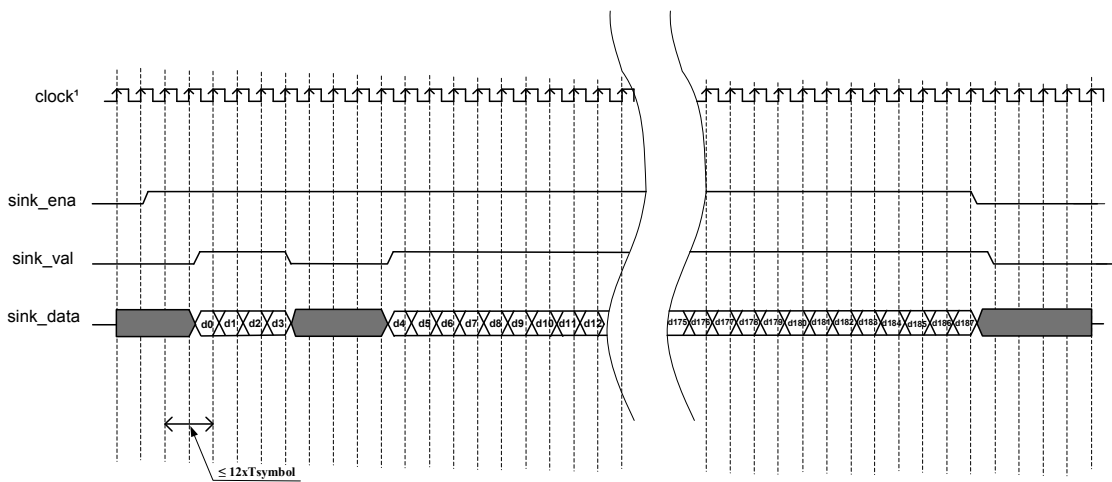


Fig.4. FEC encoder input. Timing diagram

¹ txIClk – transmitter interface clock

4.3.2. Demodulator (Receive Side)

The demodulator uses a separate clock for a data interfaces. The frequency can be between 100 and 175MHz. The same applies as in transmitter - Ethernet implementation uses 125MHz and SDH interfaces 155.52MHz.

When the user has asserted **source_ena** signal, indicating it is ready to receive data, and the demodulator has locked onto a signal, it will start to supply data on its output bus, in 188 byte bursts. It will assert **source_val** during the burst (Fig.5 below)

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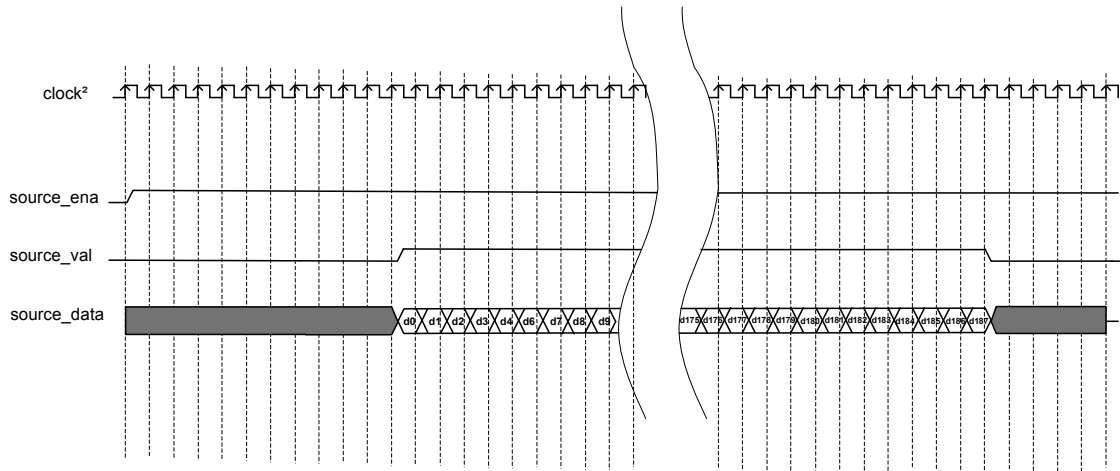


Fig.5. FEC decoder output. Timing diagram

² rxIClk - receiver interface clock

4.4. Resource Usage

Device	Parameters			Resources				Performance	
	Modulation	Roll-off %	Bandwidth min-max MHz	LEs	Memory (bits)	Multipliers	PLL	fMax, MHz	Throughput, max, Mbit/s (Msymbol/s)
EP3C55[C6]	1024QAM	18	7 - 112	44K (78%)	1.4M (59%)	272 (87%)	3 (50%)	221	890 (104)

5. Contacts

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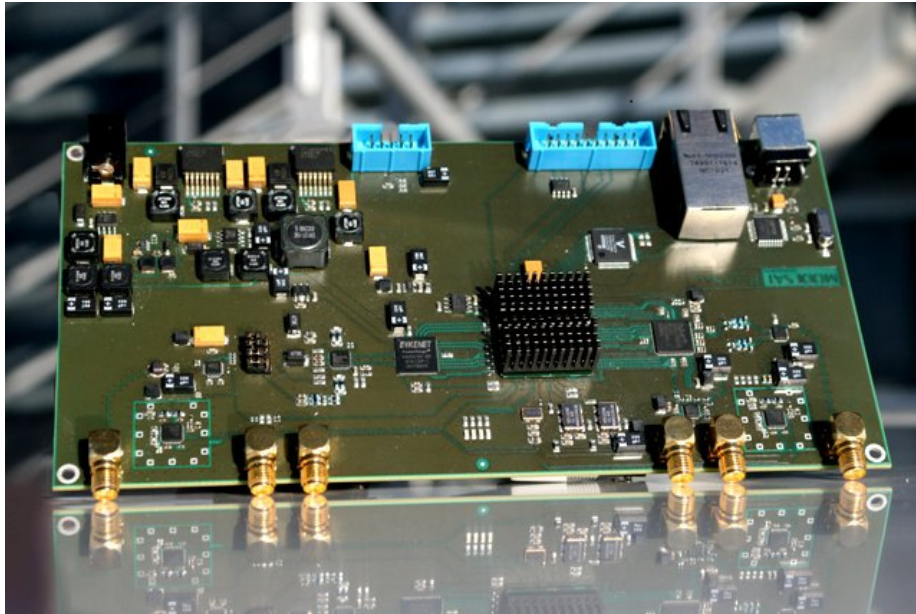
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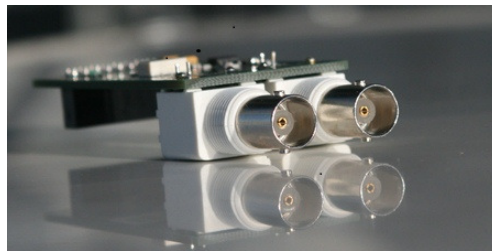
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6. EVB diagrams

6.1. EVB Main Board



6.2. TDM HDD3 daughterboard



6.3. TDM CMI daughterboard

