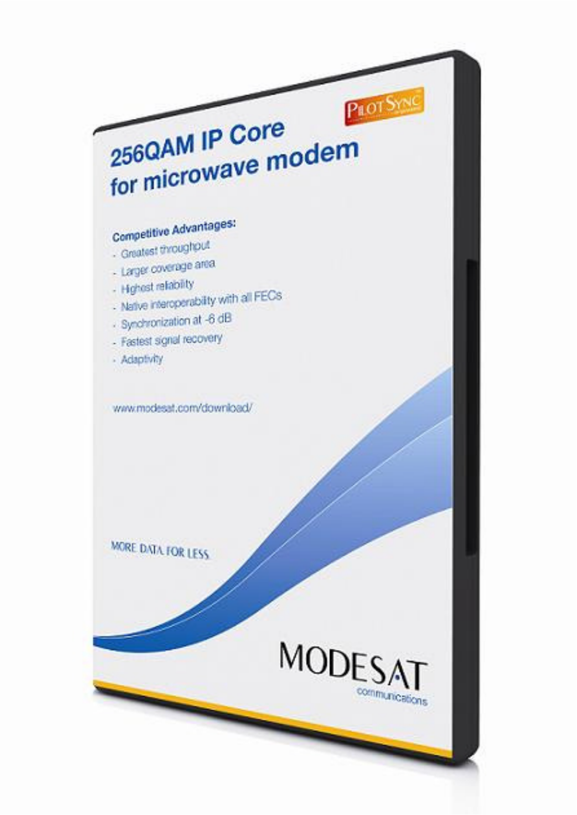
October 22, 2010 Version 3.0

Modesat Communications 256QAM Modem IP Core Product Description



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1. Overview

The Modesat 256QAM modulator / demodulator IP Core with PilotSync™ technology is designed point-to-point applications, with focus on point-to-point microwave for backhaul, broadcasting and trunking segments. The 256QAM modem IP Core is a single carrier QAM modem. The 256QAM modem IP Core can be evaluated and tested on Modesat RDK-EP3C40 Evaluation Board (EVB) based on the Altera CYCLONE III EP3C40 FPGA. For evaluation purposes Modesat offers limited functionality 256QAM Evaluation IP Core, which is provided to a customer together with RDK-EP3C40 evaluation platform.

The Modesat 256QAM Evaluation IP Core allows evaluation of the Modesat PilotSync™ based technology in nominal configuration, including Reed Solomon FEC. This modulation and coding scheme is coded into the 256QAM Evaluation IP Core application and uploaded onto the FPGA by means of the USB Blaster download cable.

The EVB with 256QAM Evaluation IP Core is intended to be used in pairs in back to back mode in order to evaluate and demonstrate performance over a full duplex communications link. IF loop mode is also possible using a mixer and LO to match the IF input and output frequencies of the EVB. User data can be generated internally or externally. In the case of externally generated data, the data interface is provided by an Ethernet, which is integral to the EVB, alternatively by a CMI or HDB3 extension board that plugs into the extension port on the EVB.

2. Features

The main features of the 256QAM IP Core are listed below:

- I/Q baseband, complex IF or real IF interface
- Input and output carrier frequencies are freely software configurable
- Transport stream is a multiplex of SDH, PDH and Ethernet data sources
- Modulation: QPSK to 256QAM (with adaptive switching)
- Roll-Off factor: software configurable 16-25%
- Bandwidth: software configurable 7 to 112MHz
- Symbol rate: software configurable 5-104 MSym/s
- Includes PilotSync™ technology
- FEC Reed-Solomon encoder/decoder 204,188
- Interleaver/Deinterleaver depth: I = 12
- Configuration via 8bit parallel host interface
- Single external analogue loop for AGC 18 bits
- Input from ADC: 11-12 bits (1 or 2 (I/Q) channels)
- Output to DAC: 10-16 bits (1 or 2 (I/Q) channels)
- Adaptive Equalizer in the receiver channel: 23 complex taps
- Modem master clock / sampling rate: single, fixed 200 or 210MHz XO clock source
- Shape Filter: Root-Raised-Cosine with 28 x N taps

  - N is the interpolation and decimation coefficient, in the case of 28MHz channel bandwidth, N=4 and the total number of taps is 112 in each channel with 12 bit coefficients in RX and 9-12 bit coefficients in TX channels
- Internal random data generator: PRBS generator with period of 2^{23} -1
- Internal BER tester

3. Supported data rates

The maximum supported transport stream data rate can be calculated according to the following formula:

*Fdata = Fsym * <bits per symbol> / <coding overhead> / <framing overhead>*

Where:

- Coding overhead is 1.0851 for Reed-Solomon 188/204 coding
- Framing overhead is 1.007

Depending on the target customer modem realization, a „wayside channel" can be defined, that reserves a part of data bandwith and makes it available on a separate data interface.

Example data rates:

Modulation	Bandwidth	Symbol rate	Data rate
256QAM	28MHz	24.3 MHz	177.9 Mbit/s
128QAM	28MHz	24.3 MHz	155.7 Mbit/s
256QAM	56MHz	48.6 MHz	355.8 Mbit/s
128QAM	56MHz	48.6 MHz	311.3 Mbit/s
256QAM	112MHz	97.2 MHz	711.6 Mbit/s
128QAM	112MHz	97.2 MHz	622.6 Mbit/s

With 200MHz master clock frequency and 200MHz MSPS ADC, symbol rates up to 99.995 MHz can be used (and its $1/2^n$ fractions). For symbol rates above and equal to 100/50/25/... a 210MHz master clock oscillator and consequently a 210MSPS ADC must be used.

4. Functional Description

4.1. Block Diagram

The functional block diagram below shows all functionality that is implemented in the FPGA, the IP modem core part comprises functionality in the central part of the figure 1.

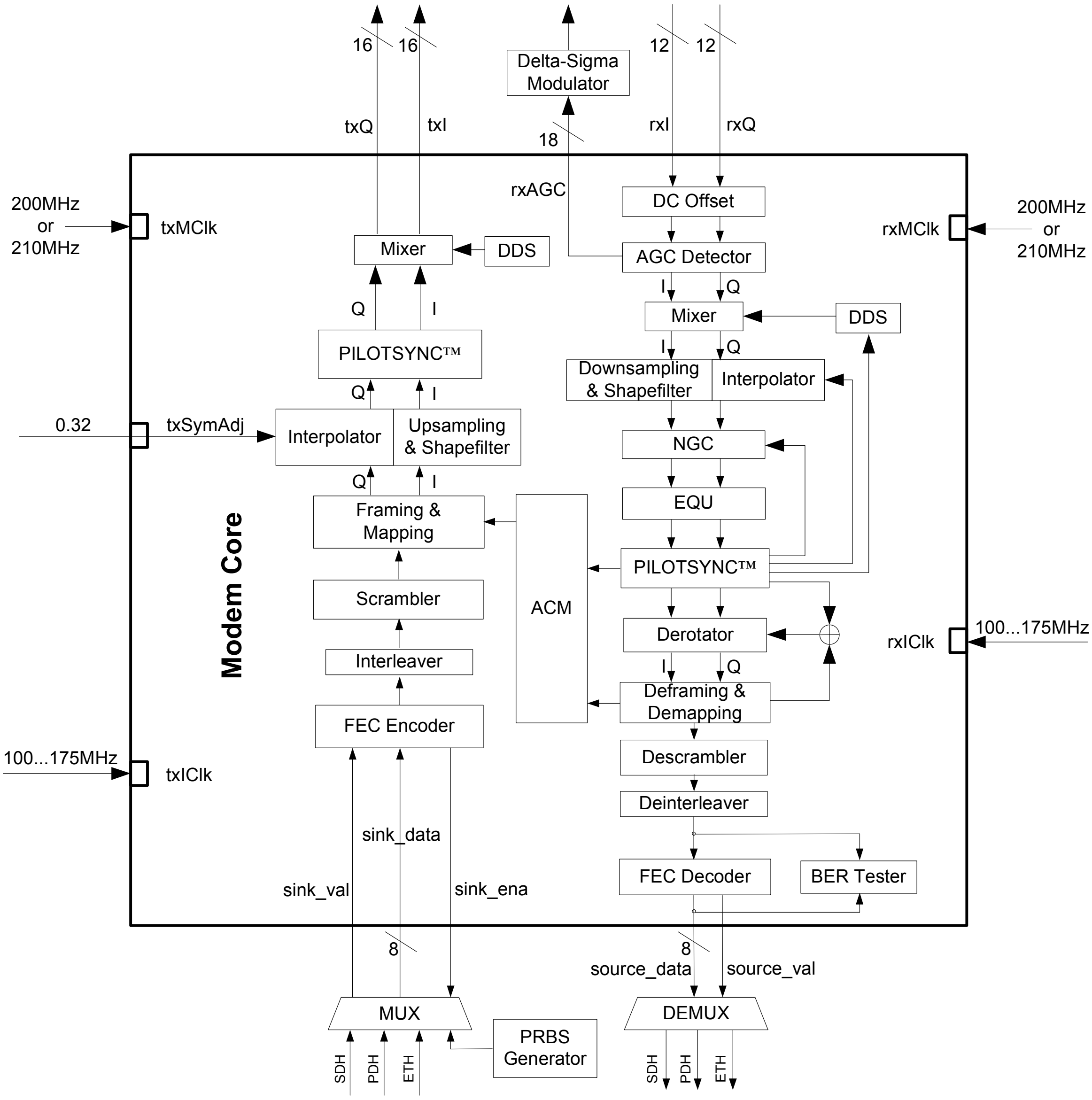

Fig.1. 256QAM IP Modem Core

4.2. 256QAM IP Modem Core Description of Operation

4.2.1. Modulator input bus and framing logic

The modulator core works on the basis of a fixed frequency master clock that represents the output sample rate and an interface clock on which the data interfaces are based. The master clock should be generated by a fixed frequency XO and it must have a frequency at least 2x higher than the highest symbol rate the modem should support. A 200MHz master clock allows symbol rates up to 100MHz-50ppm. To achieve higher symbol rates like 104MHz, a 210MHz XO can be used.

The modulator input data bus is essentially a subset of an Avalon-ST input bus to the Reed-Solomon FEC encoder. The timing of data transfers is however governed by the physical layer framing logic. Data transfers take place in the form of 188 byte packets, which form the data part of a Reed-Solomon codeword. The number of these 188 byte packets that are collected together to form one physical layer frame depends on the modulation used. When QAM256 is used, the physical layer frame contains 16 R-S codewords. When QAM16 is used, it contains 8 R-S codewords, in order to maintain the same physical layer frame length in symbols. All physical layer frames start with a 23 symbol header.

If it is desired that the main Reed-Solomon encoded data channel only uses a portion of the physically available bandwidth, the framing logic can include a number of „wayside“ symbols in every physical frame. This forms a separate uncoded channel (“wayside channel”), which represents the available excess bandwidth. The number of wayside symbols per physical frame can be configured with 0,5 symbol accuracy, but the number of symbols that can actually be used for wayside data traffic can only be an even multiple of 16 symbols. I.e. if the user wants to use QAM256 modulation with 469 symbols of wayside traffic per physical frame (typical for Reed-Solomon encoded STM-1 bitstream modulated into a 28MHz channel using 18% roll-off factor), the structure of the physical frame will contain:

23 symbols for PL header
3264 symbols for 16 R-S codewords
464 symbols of wayside traffic available for client use
5 dummy, unusable wayside symbols

The number of wayside symbols can be configured via the registers accessible over the host interface bus. Refer to Fig.2.

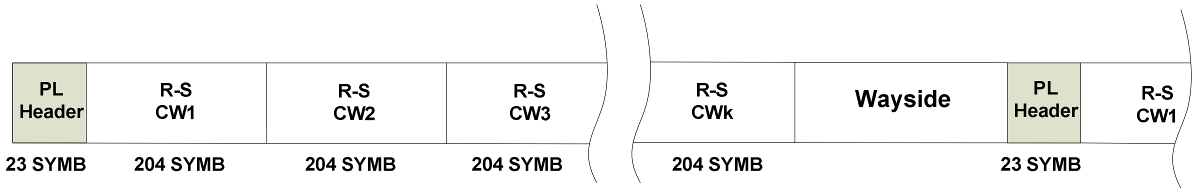

Fig.2. Structure of physical frame.

4.2.2. Mapping

Reed-Solomon encoded and scrambled stream of bytes is sliced into symbols, each representing 8 or less bits, depending on the modulation used. The resulting unmapped symbols are then mapped onto actual constellations using a ROM-based mapper. The modulation and constellation map used can be configured via the registers accessible over the host interface bus.

4.2.3. Upsampling and shaping filter

The modulated symbol stream will pass through a polyphase oversampling filter that also acts as a root-raised-cosine filter. The oversampling ratio (which determines the channel bandwidth) can be configured via the registers accessible over the host interface bus.

The relative (with respect to symbol rate) frequency response of this composite filter is equivalent to the 28 tap root-raised-cosine filter, which is itself a 2x oversampling filter. The output of this filter is then oversampled by an arbitrary factor which is for example 4.13x for 28MHz bandwidth operation with a 18% roll-off RRC filter.

4.2.4. Modulator output and direct IF mixer

At its output, the modulator has a complex IF mixer with an associated DDS local oscillator, the base frequency of which is configurable via the registers accessible over the host interface bus. The I and Q output channels of the modulator have 16 bit resolution. In order to use the I and Q outputs as baseband outputs, the mixer local oscillator DDS needs to be programmed to 0 Hz. The output can also be programmed for low-IF and complex-IF applications. For real-IF applications only I or Q outputs can be used.

4.2.5. Demodulator ADC input

The demodulator core works on the basis of a fixed frequency master clock that represents the input sample rate and an interface clock on which the data interfaces are based. The master clock should be generated by a fixed frequency XO and it must have a frequency at least 2x higher than the highest symbol rate the modem should support. A 200MHz master clock allows symbol rates up to 100MHz-50ppm. The master clock of the receiver is generally supplied by the ADC, in parallel with its data bus. The clock that drives the ADC is usually the same 200MHz or 210MHz clock used as the transmitter master clock.

Data is fed into the demodulator on the I and Q channels, each having at most 12 bits of resolution. When the demodulator is used for direct sampling of a real IF signal, then only one of them is used.

4.2.6. Static complex baseband equalizer

The baseband equalizer is there to correct for the predictable channel frequency and phase response distortions caused by the imperfections in modulators, demodulators and ones that are caused by the design of analogue filters. It is mainly necessary for operation at wider bandwidths. Its coefficients are set through the host registers.

4.2.7. DC offset cancellation circuit

This circuit corrects the DC offset that stems from imperfections in circuit design and also corrects the near-DC fluctuations caused by the effects of AC coupling of baseband I and Q channels.

4.2.8. Demodulator analogue AGC detector and loop

The analogue AGC loop aims to keep the signal level at the input of the ADC low enough that it does not clip. The AGC digital loop filter output has 18 bits of resolution and is generally used for driving a second order delta-sigma modulator that forms a 1bit DAC. The output of this DAC is used to drive an analogue VGA.

4.2.9. Direct IF sampling mixer

The demodulator input I and Q channels are always fed into a complex mixer together with a local oscillator signal that is produced by a DDS. During baseband I and Q operation, the base frequency of this DDS is configured to be 0Hz. When direct IF sampling (real or complex) is desired, the frequency of this DDS is configured to equal the RX IF frequency via the registers that are accessible over the host interface bus.

4.2.10. Downsampling and shaping filter

The baseband I and Q channel data are fed into a polyphase downsampling filter that also acts as a root-raised-cosine filter. The downsampling ratio (i.e. the channel bandwidth) can be configured via the registers accessible over the host interface bus.

The relative (with respect to symbol rate) frequency response of this composite filter is equivalent to that of the 28 tap root-raised-cosine filter.

4.2.11. NGC

The NGC (numerical gain control) is an active element of the secondary automatic gain control loop which aims to keep the signal level at the input of the equalizer within acceptable range.

4.2.12. Equalizer

The equalizer locks onto the physical layer framing structure and measures the impulse response of a channel based on physical layer frame headers. A DSP within the equalizer then calculates the filter coefficents necessary to counter the frequency and phase response non-linearities of the channel and a 23 tap complex FIR filter processes the baseband I and Q channels to get the clean signal.

4.2.13. Derotator

Equalized I and Q channels are fed into a derotator, which is essentially a complex mixer with a 0Hz local oscillator DDS. The phase of this local oscillator is controlled by the demapper.

4.2.14. PilotSync™ synchronizer

The synchronizer extracts and analyzes the pilot tones present in the signal and produces several control signals, including:

- symbol (ADC) clock control signal that adjust the downsampling ratio of the Rx channel filter
- carrier frequency control signal that drives the baseband demixer
- level adjustment signal that drives the NGC

Parameters of all filter loops can be adjusted via the registers that are accessible over the host interface bus.

4.2.15. Deframing, demapping and demodulator data output

The deframing and demapping block demaps the received signals into binary symbols based on a constellation chosen via the host interface registers and slices them together to form a stream of 8- bit bytes. This bytestream is then fed into the Reed-Solomon decoder in the form of 204 byte codewords. The output of the Reed-Solomon decoder forms the output of the PilotSync™ modem. Only the 188 bytes of corrected data is output per every codeword. Every 188 byte payload packet is sent out as a single burst, at the master clock rate of the demodulator.

Deframing logic also extracts the side channel from the main channel and outputs it on a separate data bus. The side channel is presently not FEC encoded.

Demapping also produces control signals to adjust the operation of several parts of the receiver.

4.2.16. Adaptive Coding and Modulation (ACM) Module

The Modesat 256QAM IP Core physical layer framing structure includes a highly guarded, low bitrate service channel, which is used by ACM module for transmitting information about line conditions (from receiver to transmitter) and messages used for synchronizing modulation changes (from transmitter to receiver). ACM module collects information about line conditions and transmits it to the transmitting modem using the service channel facilities provided by the physical layer framing module. From the service channel that is received by the deframing module, ACM module receives information from the receiving modem to which this modem is transmitting data to. Based on signal condition information it receives, it switches the modulation scheme used by the mapper.

4.2.17. FEC Reed-Solomon encoder/decoder

The Modesat 256QAM IP Core uses the Reed-Solomon Compiler from Altera to apply FEC encoder and decoder in Standard encoder and Full bit error decoder configuration.

The Reed-Solomon encoder and decoder interfaces are based on the Avalon-ST interface specification. Alternative FEC options can be provided upon the request of the customer, however using other FECs will increase resource requirements.

4.3. IP Modem Core Input and Output signals

Fig. 3 below shows a high level view of the main blocks that comprise the IP Modem core, with focus on the input and output signals. These signals are further described in the paragraphs below.

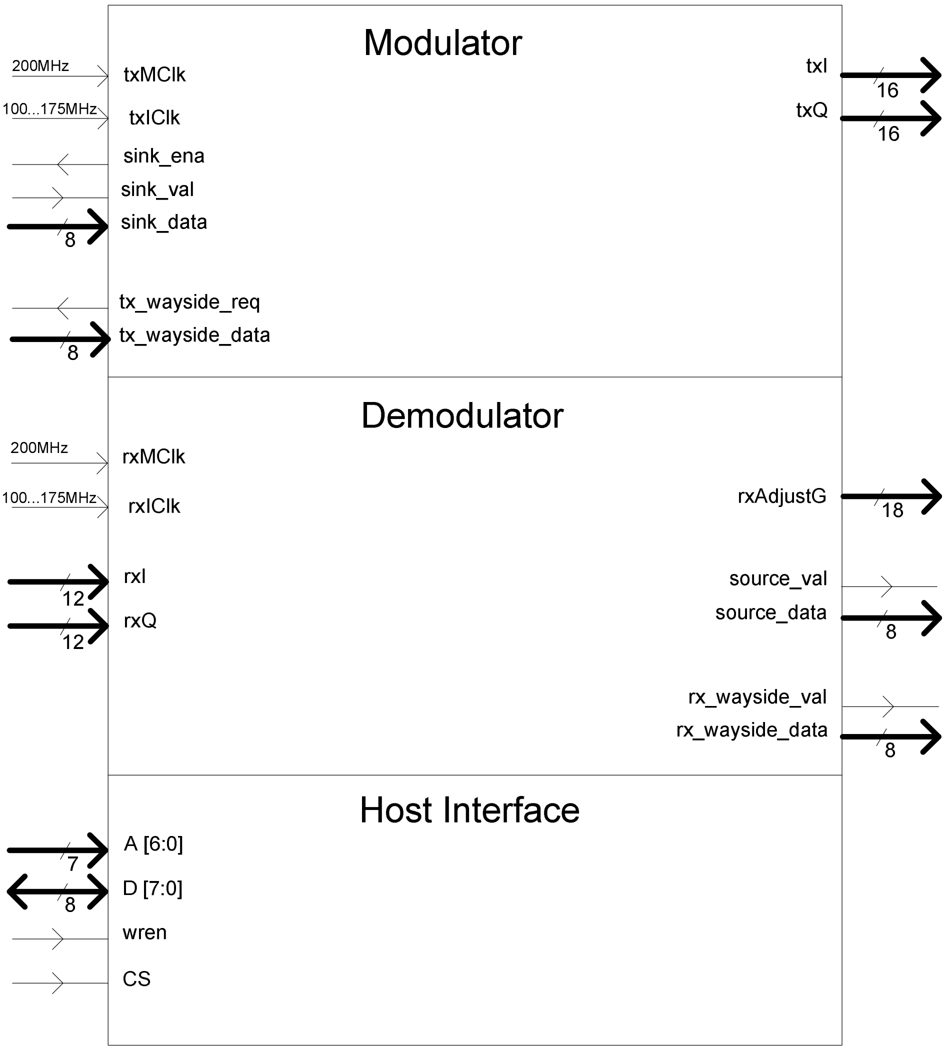

Fig.3. Modem Core.

4.3.1. Modulator (Transmit Side)

The modulator uses a separate clock for a data interfaces. The frequency can be between 100 and 175MHz. Ethernet implementation would use 125MHz as an interface clock, for SDH interfaces, 155.52MHz would be most convenient.

The **sink_ena** signal indicates that a modem is ready to receive a packet of data. Refer to Fig.4. FEC encoder input - Timing diagram. The packet size is 188 bytes, i.e. one Reed-Solomon codeword before encoding. An asserted **sink_val** indicates that **sink_data** bus represents a valid data byte. The first byte must be provided within 12 symbol time periods (48 or 96 clock periods) of **sink_ena** going high. Data transmission on the sink_data/sink_val bus does not need to be continuous, it can be interrupted at any time by lowering **sink_val**. The average byte rate must however be at least equal to the transmission bandwidth.

After the last byte of a 188byte packet has been received by the modem, it lowers the **sink_ena** signal, indicating that it is not ready to accept any more data. It will assert **sink_ena** again when there is enough room in the transmit buffer.

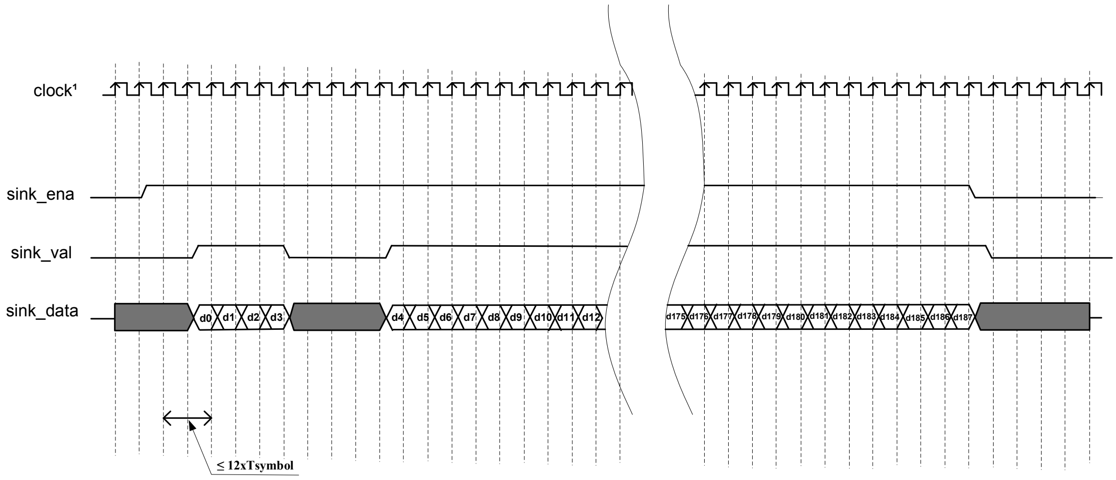

Fig.4. FEC encoder input. Timing diagram

[1] txIClk – transmitter interface clock

4.3.2. Demodulator (Receive Side)

The demodulator uses a separate clock for a data interfaces. The frequency can be between 100 and 175MHz. Ethernet implementation would use 125MHz as an interface clock, for SDH interfaces, 155.52MHz would be most convenient.

When the user has asserted **source_ena** signal, indicating it is ready to receive data, and the demodulator has locked onto a signal, it will start to supply data on its output bus, in 188 byte bursts. It will assert **source_val** during the burst. Refer to Fig.5. "FEC decoder output. Timing diagram."

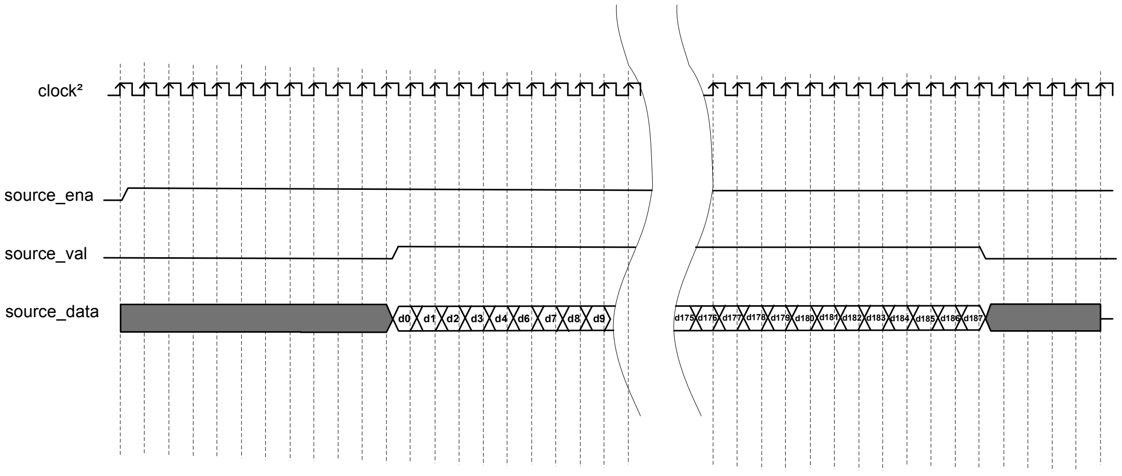

Fig.5. FEC decoder output. Timing diagram

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[2] rxIClk - receiver interface clock

4.4. Resource Usage

Device	Parameters			Resources				Performance	
	Modulation	Roll-off %	Bandwidth min-max MHz	LEs	Memory (bits)	Multipliers	PLL	fMax, MHz	Throughput, max, Mbit/s (Msymbol/s)
EP3C40[C6]	256QAM	18	7 - 112	32 757 (83%)	1 010 304 (87%)	248 (98%)	2 (50%)	221	761 (104)

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